AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

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a circuit configured to translate instruction codes of a first instruction set on-the-fly into addresses into a microcode memory containing sequences of instruction codes of a second instruction set that emulate a functionality of the instruction codes of the first instruction set.

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said sequences of instruction codes of ~~a~~ said second instruction set generated in response to said instruction codes of said first instruction set are stored in a ~~computer readable medium~~ cache.

3. (CURRENTLY AMENDED) The apparatus according to claim ~~2~~ 1, wherein said ~~computer readable medium~~ circuit comprises a decoder configured to generate said addresses into said microcode memory.

4. (CURRENTLY AMENDED) The apparatus according to claim ~~3~~ 1, wherein predetermined sequences of said instruction codes of

said first instruction set are used to address said microcode memory.

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5. (CURRENTLY AMENDED) The apparatus according to claim ~~3~~ 1, wherein addresses into said microcode memory are generated by a look-up-table in response to said instruction codes of said first instruction set.

6. (ORIGINAL) The apparatus according to claim 1, wherein said instruction codes of said second instruction set comprise native instructions of a target processor.

7. (ORIGINAL) The apparatus according to claim 6, wherein said target processor is selected from the group consisting of MIPS, ARM, and Motorola 68K.

8. (ORIGINAL) The apparatus according to claim 3, wherein said microcode memory can be reprogrammed to support different processors.

9. (ORIGINAL) The apparatus according to claim 1, wherein said circuit is configured to format the sequences of instruction codes of said second instruction set according to an opcode format of a processor.

10. (ORIGINAL) The apparatus according to claim 1, wherein said circuit is configured to detect optimizable sequences of instruction codes on-the-fly.

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11. (ORIGINAL) The apparatus according to claim 1, wherein said circuit comprises a sequence optimization circuit.

12. (ORIGINAL) The apparatus according to claim 1, wherein said circuit comprises a native instruction sequence generator circuit.

13. (ORIGINAL) The apparatus according to claim 1, wherein said circuit is coupled between a processor and a memory system.

14. (ORIGINAL) The apparatus according to claim 13, wherein said circuit is configured to (i) directly connect said processor and said memory system during a first state of operation and (ii) during a second state of operation, communicate with said processor as though said circuit was the memory system and communicate with said memory system as though said circuit was the processor.

15. (ORIGINAL) The apparatus according to claim 1, wherein said instruction codes of said first instruction set comprise Java bytecodes.

16. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said circuit comprises a ~~hardware~~ portion of a Java virtual machine implemented in hardware.

17. (CURRENTLY AMENDED) An apparatus comprising:

means for translating instruction codes of a first instruction set on-the-fly into addresses into a microcode memory containing sequences of instruction codes of a second instruction set that emulate a functionality of the instruction codes of said first instruction set;

means for receiving said ~~instructions~~ instruction codes of said first instruction set; and

means for presenting said ~~instructions~~ sequences of instruction codes of said second instruction set.

18. (CURRENTLY AMENDED) A method for on-the-fly translation of instructions of a first instruction set into instructions of a second instruction set comprising the steps of:

(A) receiving an instruction code of said first instruction set;

(B) generating an address into a microcode memory in response to said instruction code of said first instruction set using a hardware translator, wherein said address points to a sequence of instruction codes of said second instruction set that will emulate said instruction code of said first instruction set ~~using a hardware translator~~; and

(C) presenting said sequence of instruction codes of said second instruction set.

19. (CURRENTLY AMENDED) The method according to claim 18, wherein step ~~C~~ B comprises the sub-step of:

~~(C-1)~~ selecting said ~~sequence of instruction codes of said second instruction set~~ address from a ~~microcode memory~~ look-up table in response to said instruction ~~codes~~ code of said first instruction set.

20. (CURRENTLY AMENDED) The method according to claim 19, wherein step C further comprises the sub-step of:

~~(C-2)~~ optimizing said sequence of instruction codes of said second instruction set for a particular processor.

21. (NEW) The apparatus according to claim 1, wherein said sequences of instruction codes of said second instruction set comprise one or more virtual stack references.

22. (NEW) The apparatus according to claim 1, wherein said microcode memory further comprises one or more of (i) a size for each sequence of instruction codes of said second instruction set, (ii) a value representing how many bytes an instruction uses from said instruction codes of said first instruction set, and (iii) a stack change variable indicating whether the stack increases or decreases due to said instruction codes of said first instruction set and by how much.